CENTRE FOR NANO SCIENCE AND ENGINEERING (CeNSE)

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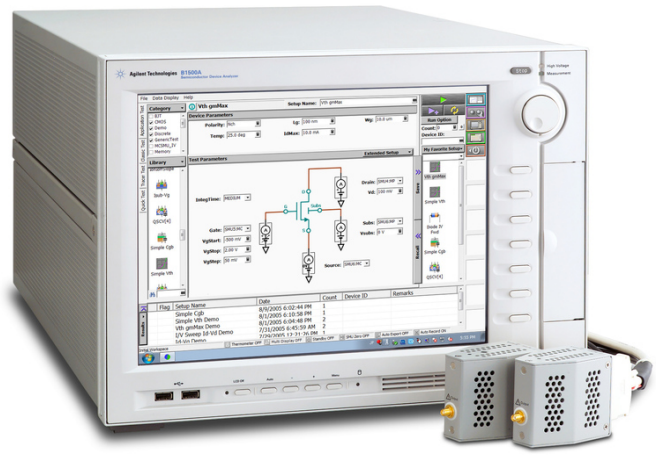
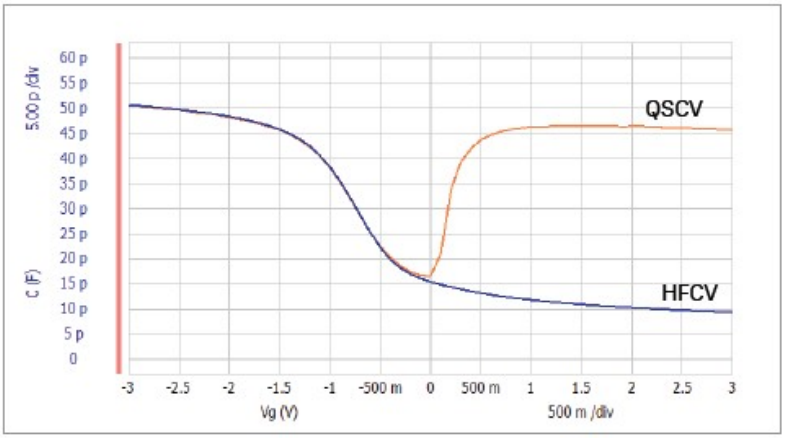
Application Note on finding Interface trap density (Dit) from QSCV (Quasi-Static Capacitance Voltage) and HFCV (High Frequency Capacitance Voltage) Measurement





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Introduction

The low frequency or quasi-static method is a common interface trapped charge measurement method. It provides information only on the trapped charge density, but not on their capture cross-sections. Before discussing characterization techniques it is useful to discuss about oxide charges.

Oxide Charges: There are four general types of charges associated with the SiO2-Si system shown on Fig 1. They are fixed oxide charge (2), mobile oxide charge (4), oxide trapped charge d(3) and interface trapped charge(1). The abbreviations of the various charges are given below. In each case, Q is the net effective charge per unit area at the SiO2-Si interface (C/cm2), N is the net effective number of charges per unit area at the SiO2-Si interface (number/cm2), and Dit is given in units of number/cm2·eV. N = |Q|/q, where Q can be positive or negative, but N is always positive.

Interface Trapped Charge (Qit, Nit, Dit)

These are positive or negative charges, due to structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or similar bond breaking processes (e.g., hot electrons). The interface trapped charge is located at the Si–SiO2 interface. Unlike fixed charge or trapped charge, interface trapped charge is in electrical communication with the underlying silicon. Interface traps can be charged or discharged, depending on the surface potential. Most of the interface trapped charge can be neutralized by low-temperature (~450◦C) hydrogen or forming gas (hydrogen/nitrogen mixture) anneals. This charge type has been called surface states, fast states, interface states and so on. It has been designated by Nss , Nst and other symbols in the past.

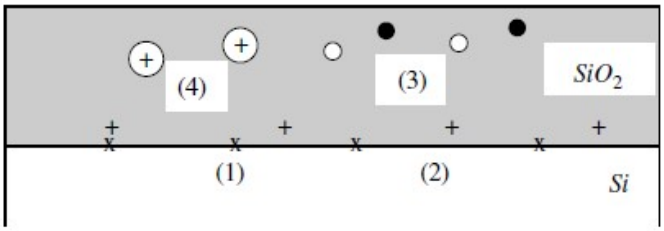


Figure1. Charges and their location for thermally oxidized silicon. [1]

Effect of Interface Traps and Oxide Charge on Device Characteristics

The presence of oxide charges and interface traps has three major effects on the characteristics of devices. First, the charge in the oxide, or in the interface traps, interacts with the charge in the silicon near the surface and thus changes the silicon charge distribution and the surface potential. Second, as the density of interface trapped charge changes with changes in the surface potential, it gives rise to an additional capacitance component in parallel with the silicon capacitance C_{si} . Third, the interface traps can act as generation-recombination centers, or assist in the band-to-band tunneling process, and thus contribute to the leakage current in a gated-diode structure. These effects are discussed more quantitatively below.

To analyze the interface state, the quasi-static capacitance voltage (QSCV) [1] and HFCV measurement technique has been the most popular method. The AC signal-based high frequency capacitance voltage (HFCV) measurement (about up to 1 MHz range) is widely used for the new materials and devices characterization, however the interface state analysis cannot be evaluated only by the HFCV measurement, because the slow interface state in-between two materials does not respond to the high frequency AC signal of HFCV.

To analyze such slow state traps, the QSCV measurement technique has been widely used, which is effective for capturing a slow frequency behavior as shown in Figure 1. The QSCV measurement uses linear DC ramp sweep or DC step voltage instead of an AC signal, and needs very low current measurement technique. It is a unique measurement method, and it is very important to understand measurement knowledge and know-hows for performing the measurement appropriately.

This application note discusses the key points in the QSCV measurements including the issues, know-hows and tips when performing the QSCV measurements using the Keysight B1500A Semiconductor Device Analyzer/EasyEXPERT software. The following topics are covered in this application note.

Basics of QSCV measurement.

1) Keysight B1500A QSCV solution

2) Set-up and tips for QSCV measurement by the Keysight B1500A

3) Dit calculations and graph plots

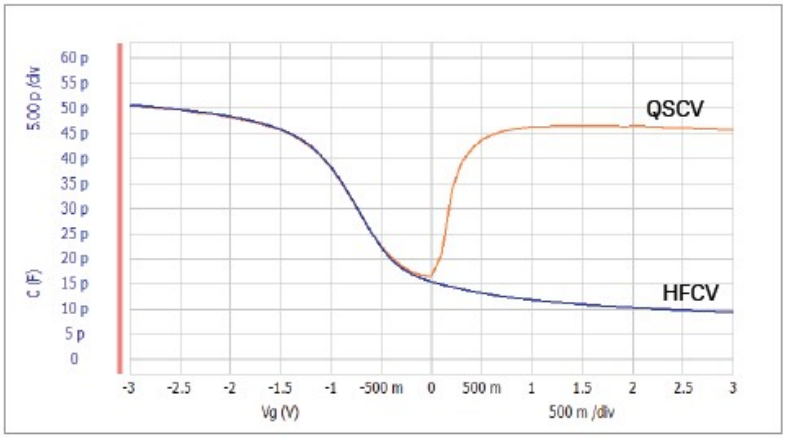


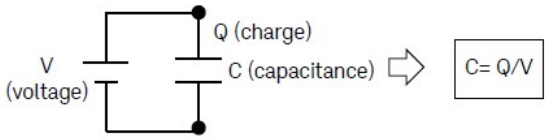
Figure2. QSCV capture the slow response that cannot be measured by HFCV [2]

Basics of QSCV Measurement

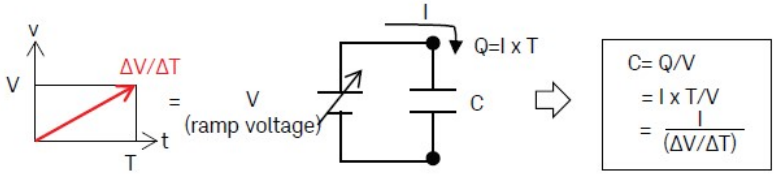
The QSCV measurement seeks the capacitance value by using the basic relation-ship between current I, voltage V, capacitance C and charge Q as shown in Figure 3. Although they are basically the same, there are two basic formulas, according to the focused variables.

Figure 3(a) shows a basic formula of C=Q/V. From this formula, the capacitance can be obtained as the function of the voltage step and the amount of the charge applied by the voltage to capacitor.

Figure 3(b) shows another formula, which is C=Q/V=IT/V=I/(V/T). The total amount of the charge Q can be expressed by the current integrated for a period of time T as Q= IT. From this formula, the capacitance can be obtained as the function of current I, voltage V and time T. Here, the V/T equals to the voltage ramp rate, so the capacitance can be obtained by the current and voltage ramp rate finally. In the following sections, two basic QSCV measurement methods by using these formulas are introduced.



(a) Basic formula of C, Q and V



(b) Basic formula of C, I, V and T

Figure3. Basic formula for QSCV measurement [2]

Linear voltage ramp

The linear voltage ramp method is a traditional measurement method of the QSCV since its start in the late 60‘s. It uses the linear voltage ramp as shown in Figure 3(b). This has been a very common method, because it simply applies the voltage at a fixed ramp rate (ΔV/ΔT) and measures the current. Unlike the step V method described later, it is not necessary to consider and control the timing precisely for the ΔQ integration.

However, some devices may have the leakage current such as electron tunneling through the gate dielectric or p-n junction. In this case, the leak current is also measured as a part of the current I in the Q= I/(V/T) formula. Because the leak current is not related to the traps, the interface state cannot be analyzed accurately for such devices as the result.

Step voltage method

The step voltage method measures the capacitance by using the formula of C=Q/V as shown in Figure 4. The amount of the charge ΔQ is obtained by the relationship of step voltage ΔV, transient current, and time. The measurement time (integration time) must be set to cover all the transient charge current to obtain the ΔQ accurately. This method is not only limited to single step, but it can be also performed in the voltage sweep and the ΔQ can be obtained in each step.

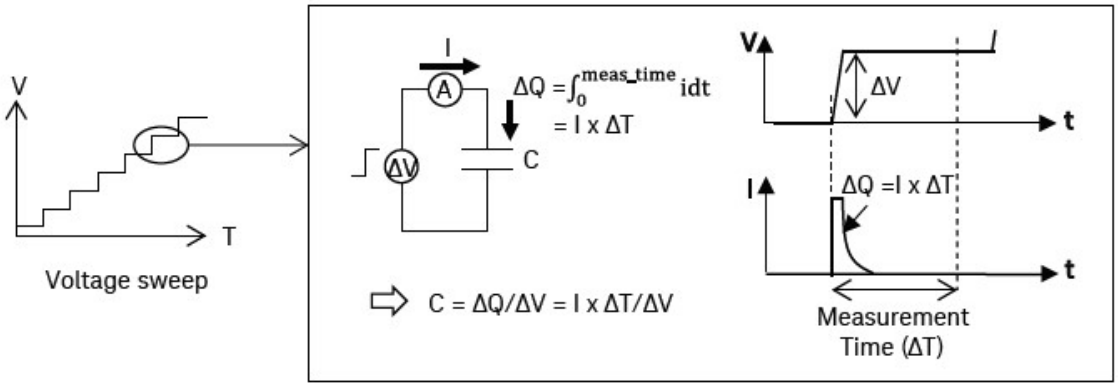


Figure4. Step voltage QSCV measurement [2]

Details of the B1500A step voltage QSCV measurement

The measurement diagram of B1500A QSCV measurement is shown in Figure 5. The basic idea of the step voltage QSCV method is the same as Figure 3, but a few more parameters are added to adapt to various devices and to sup-port advanced capabilities. The Figure 6(a) shows the entire CV sweep of QSCV measurement, and Figure 6(b) shows a magnified view of the a sweep step. More details of a QSCV measurement in a step are shown in Figure 6(c)

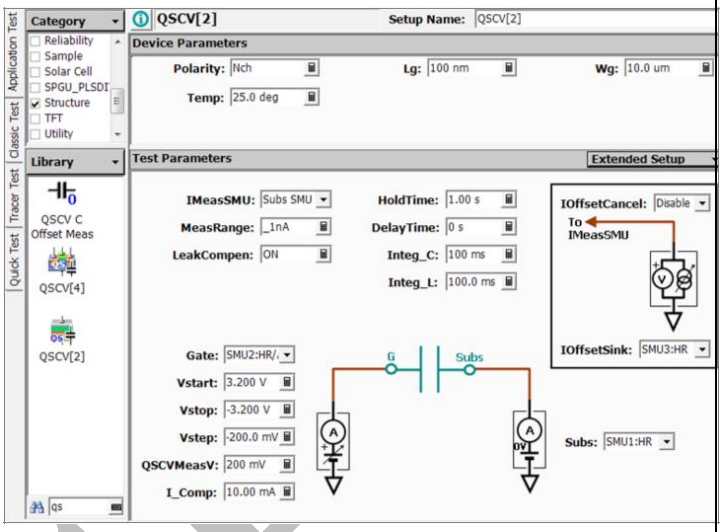


Figure5. Ready to use QSCV application test [2]

In the original idea of the voltage step QSCV method as shown in Figure 3, the QSCV measurement is performed by the step voltage of CV sweep. However, in this case, the QSCV measurement parameter (ΔV) is fixed by the CV sweep set-tings of start V, stop V and number of sweep steps. Typically, those parameters are defined by the device operating range from accumulation to inversion, and the number of points to plot the curve. So it limits the freedom to optimize the QSCV measurement parameters.

In the QSCV measurement, the ΔV of QSCV measurement can be set independently from the step voltage of the CV sweep as shown in Figure6 (b). Along the CV sweep, any same or different ΔV can be specified for QSCV measurement across each sweep step voltage. At the beginning of the QSCV measurement, the voltage is set to (sweep step voltage Vstep-n - ΔV/2). If necessary, it is possible to place the delay time to wait for the settling of charge current by CV sweep step voltage. Then the QSCV measurement is performed with ΔV from (sweep step voltage Vstep-n - ΔV/2) to (sweep step voltage Vstep-n + ΔV/2), as shown in Figure 6(c). The charge ΔQ induced by the ΔV can be calculated by measuring the current and numerically integrating the area under the current versus time curve precisely inside of the B1500A. As a result, the capacitance at each step can be obtained by the formula of C= ΔQ/ΔV along with any step voltage of CV sweep.

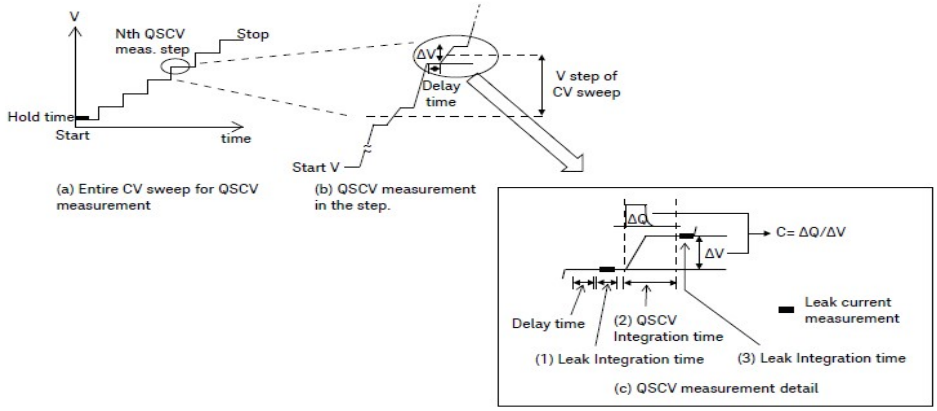


Figure6. Details of step voltage QSCV measurement [2]

Leakage current compensation:

If the device has the leakage current such as electron tunneling through the gate dielectric or p-n junction, it cannot be distinguished from the charge current for QSCV measurement. To reduce the error caused by those leakage currents, the QSCV measurement provides the advanced feature to compensate the leakage current. It measures the leakage current before and after the QSCV measurement as shown in figure 5(c), and then subtracting out the leakage current before calculating the ΔQ for the capacitance.

Since the above leakage current compensation is made by using the same current range which measures the QSCV current, the compensated maximum leak current is limited to the QSCV measurement current range. If the leak current is large, the leak current cannot be fully compensated. If the higher current range is used for the large leakage current, the QSCV measurement accuracy tends to be degraded. To resolve this challenge, the B1500A provides another leakage current compensation capability (I offset cancelation) by using additional SMU. This additional SMU is connected in parallel to force the current to cancel the large leak, enables to perform QSCV measurement in the appropriate range even with the large leak. It can be set up as shown "IOffset Cancel" in the center-right of figure 6.

QSCV offset compensation:

Offset capacitance and the leakage current can be the error (or parasitic) factors for QSCV measurement as shown in Figure 7. As well as HFCV measurement, stray capacitance between the measurement terminals is regarded offset capacitance (Coffset) to be compensated. In addition, the QSCV method calculates the ca-pacitance from the charge current, so the leakage current (I_leak) without device is also contributed to the capacitance calculation. Unless these are appropriately compensated, the QSCV result can include some measurement errors.

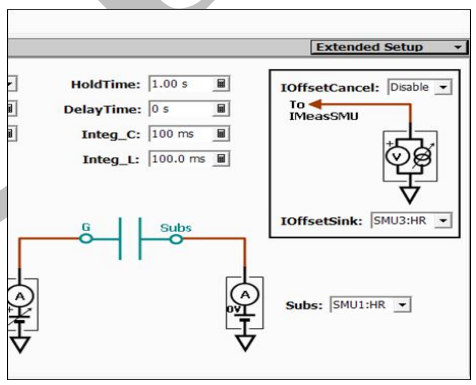


Figure7. Shows the I offset cancel apability [2]

The B1500A supports both of these measurements to determine the offset capacitance and the leakage current while the test terminal is open. The I-leak offset current is also converted to offset capacitance C(I_leak) using the QSCV measurement parameters, and generates total offset capacitance Cmo in addition to Coffset. The Cmo is stored and automatically subtracted from subsequent QSCV measurements (Cm), and you can get the compensated result.

The offset measurement GUI is shown in Figure 8. The current measurement SMU (IMeasSMU) and the current measurement range (MeasRange) have to be the same for accurate Coffset compensation.

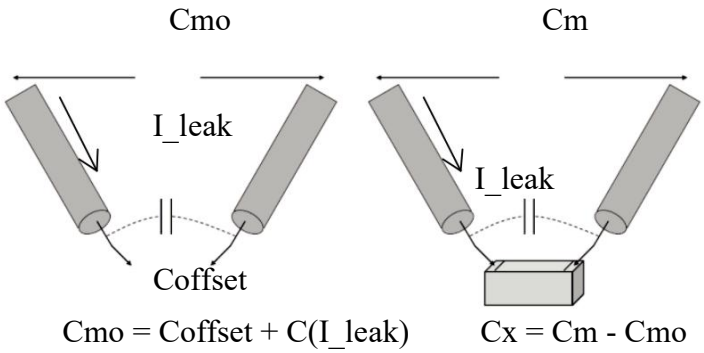


Figure8. offset capacitance compensation.

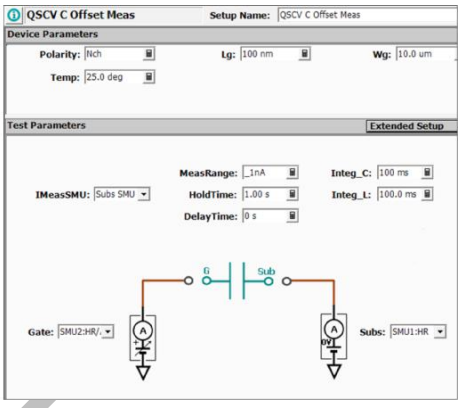


Figure9. offset capacitance measurement GUI.

Parameters in the application test

In the B1500A QSCV application test, you can control the following parameters in the GUI in Figure 9.

— CV sweep setup parameters:

Start V, Stop V, Step V: CV sweep parameters. Refer to Figure 5.

I_comp: Current compliance of SMU.

HoldTime: Wait time before starting the CV sweep at the first bias voltage. Refer to figure 5(a).

— QSCV measurement setup parameters:

IMeasSMU: SMU to measure the charge current for QSCV.

MeasRange: Current range of SMU to measure the charge current for QSCV.

Integ_C: Integration time for ΔQ for QSCV. Refer to Figure 5(c).

QSCVMeasV: Step voltage ΔV for QSCV. Refer to Figure 5(c).

DelayTime: Delay time before starting the QSCV measurement at each CV sweep step. Refer to Figure 5(c).

— Leakage current compensation setup parameter

LeakCompen: Switch to enable/disable the leak compensation.

Integ_L: Integration time for leakage current measurement.

— I offset cancelation capability

IOffsetCancel: Switch to enable/disable the I offset cancel capability

IOffsetSink: Specify the SMU to connect in parallel to the "IMeasSMU“

In the following section, the setup method of these parameters is discussed.

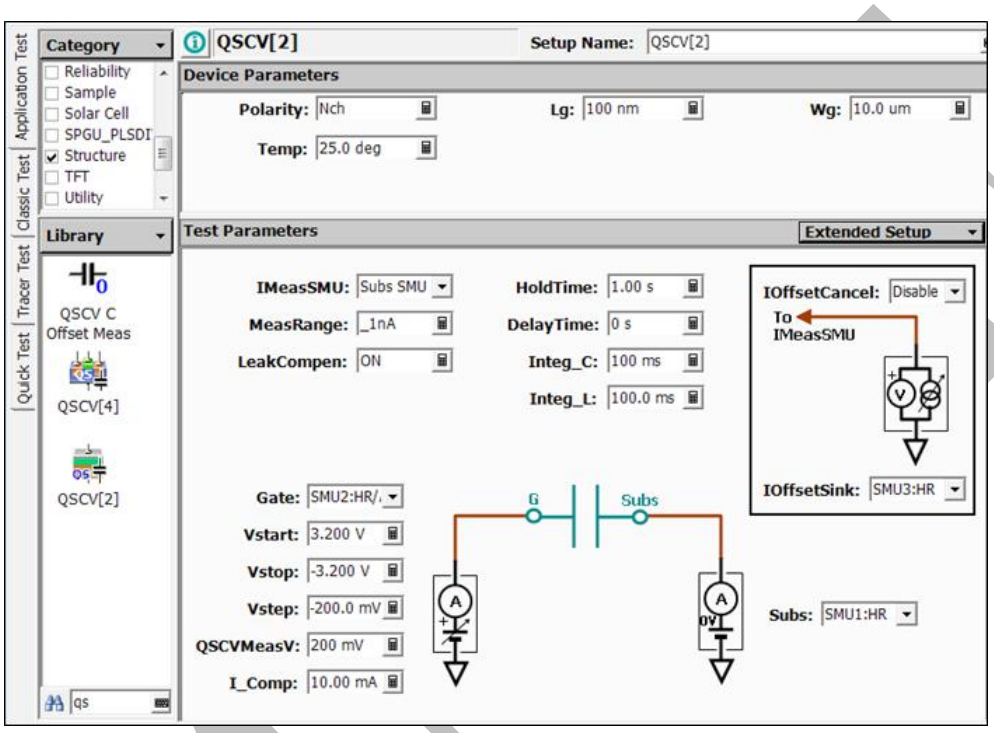


Figure10. GUI and setting parameters for QSCV measurement [2]

Set-up and Tips for QSCV Measurement by the B1500A

This section provides several useful information to setup QSCV parameters and tips for accurate measurement to meet in various situations. There is a deep relation between the integration time setting, current range setting, leakage current setting and the capacitance value in the QSCV measurement, and the explanation starts from these relations.

Typical steps for successful QSCV measurement setups

The step voltage QSCV test setup can be made easier if the measurement starts from the DC and HFCV measurement as shown in Figure 10. The B1500A supports the seamless measurement among the IV and QSCV measurement by SMU and HFCV measurement by the CMU (Capacitance Measurement Unit) with the optional SCUU (SMU CMU Unify Unit) as shown in Figure 11. This enables you to perform accurate HFCV and QSCV measurement quickly and effortlessly. Through the DC and HFCV measurements, the following useful information can be obtained for QSCV measurement.

DC measurement to know leakage current:
DC leakage current information is useful for determining the minimum QSCV measurement range. It can also be useful for determining if the DC leak compensation function is used.

HFCV measurement to know maximum capacitance value:
If the capacitance value can be known roughly in advance, you can set the various parameters such as QSCV measurement range, step voltage and integration time smoothly. This is already described in the user manual of B1500A.

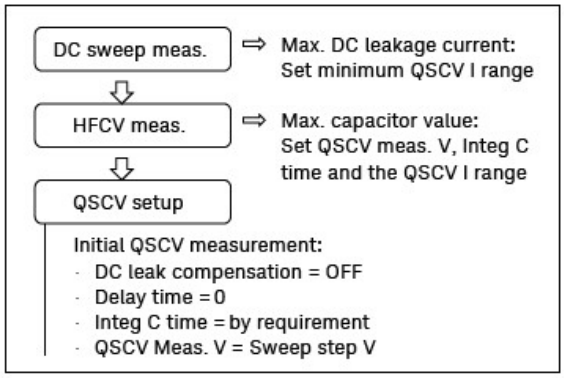


Figure 10. Typical QSCV test setup flow[2]

Typical steps for successful QSCV measurement setups

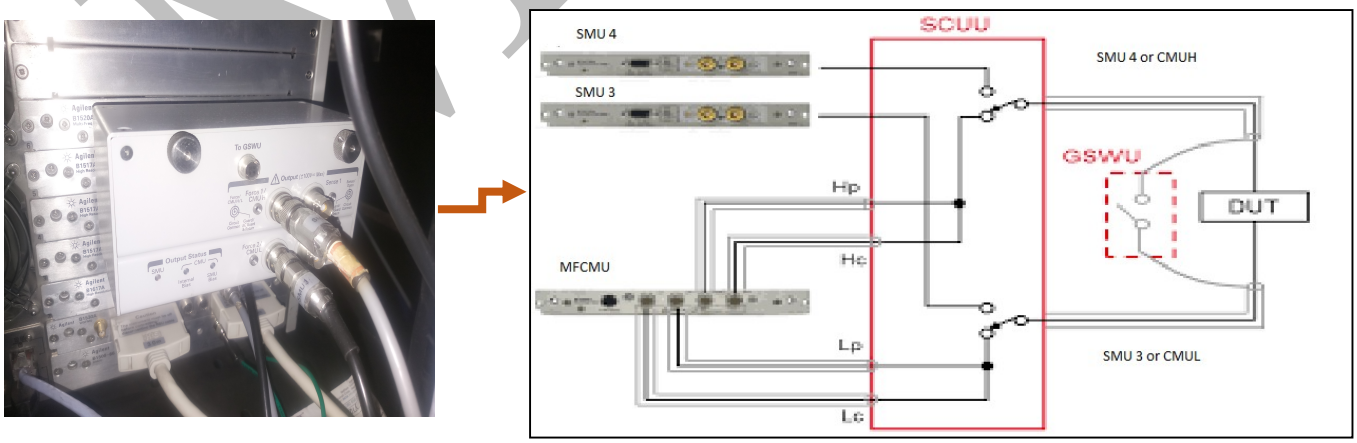


Figure 11. SCUU diagram [2]

How to set the QSCV measurement parameters

The following section provides the information how to set the measurement parameters appropriately.

— Set longer QSCV integration time than the graph of maximum measurement value:

The graph of maximum measurement value in the user's guide shows the measurement limitation of the maximum capacitance that can be measured at the combination of parameters, as shown in Figure 12 and 13 as the examples. According to your capacitance value, this graph provides the good starting point of C integration time (Integ_C) at specific ΔV. For example, if the 1 nF capacitance is measured at 0.1 V step, the graph shows the 100 ms as the minimum C integra-tion time. So set the C integration time larger than this value. If the QSCV measurement fails, the compliance state "C" or overflow status "V" is shown in the data status, and then try a longer integration time.

— Start the measurement range equal to or larger than 1 nA range:

The 1 nA and higher ranges allow larger capacitance measurement, so it is recommended to start from 1 nA range. As shown in the Figures 12 and 13, the maximum capacitance value is a function of ΔV as well as C integration time. If the ΔV is from 0.1 V to 0.2 V, the 1 nA range allows up to 10 nF, but 10 pA/100 pA allows up to 10 pF approximately at 1 s C integration time. If the capacitance is known small appropriately for 10 pA/100 pA ranges, of course those ranges can be used. After starting the parameter combination on this graph, and then adjust those parameters according to the device characteristics.

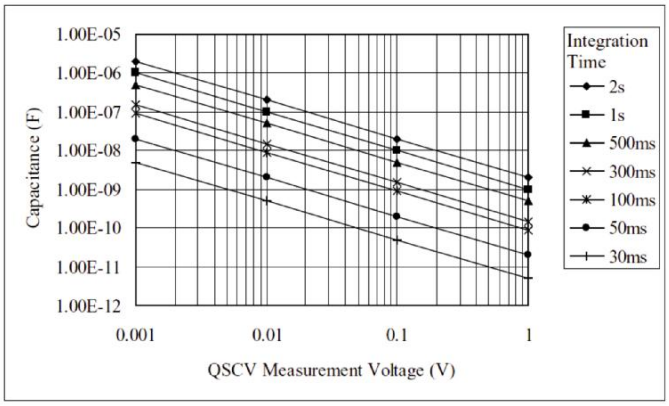


Figure 12. Maximum measurement value by parameter combination (1 nA range) [2]

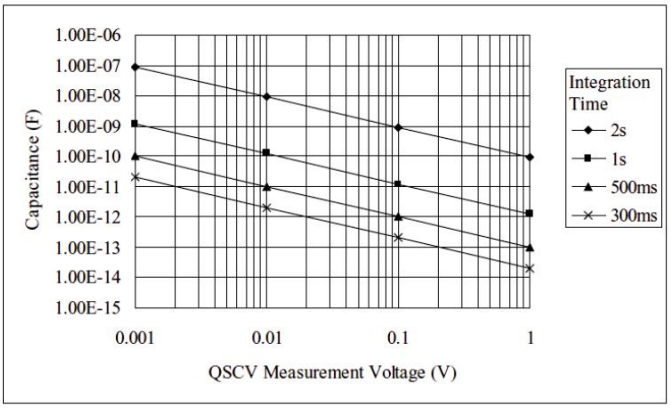


Figure 13. Maximum measurement value by parameter combination (10 pA and 100 pA ranges) [2]

— Additional notes to measure the device with slow interface state:

When measuring the device with slow interface state, pay more attention to the C integration time. Due to the slow interface state, the value of device capacitance can be shifted during the measurement, and the charge current is slowly settled down. To characterize the device with accurate ΔQ, it is important to integrate the charge current enough by the end of the settling, which has its time constant. To integrate the charge current by settling within about 5 %, the C integration time needs to be longer than approximately three times the time constant of the QSCV response, in the time constant matter. For most cases, the integration time from 5 s to 10 s is enough at maximum, in case the leak compensation is disabled.

When the leak compensation is enabled for a leaky device, adjusting the C integration time becomes more important to fully integrate the charge current. If a longer C integration time is necessary, adjusting the L integration time sometimes provides better results. To obtain a satisfactory result, it may be necessary to adjust the parameters by try and error of repeat measurements by comparing the data.

When the CV sweep step is larger than the ΔV of QSCV measurement, adjust the delay time as well. The charge current of slow state caused by the CV sweep might not be settled down yet at the QSCV measurement.

How to use the leak compensation

The step voltage QSCV test setup can be made easier if the measurement starts from the DC and HFCV measurement as shown in Figure 10. The B1500A supports the seam-less measurement among the IV and QSCV measurement by SMU and HFCV measure-ment by the CMU (Capacitance Measurement Unit) with the optional SCUU (SMU CMU Unify Unit) as shown in Figure 11. This enables you to perform accurate HFCV and QSCV measurement quickly and effortlessly. Through the DC and HFCV measurements, the following useful information can be obtained for QSCV measurement.

— Enable the leak compensation for leaky device:

The QSCV measurement is very susceptible to the leakage current of the device, and it is important to know the level of the leakage current. The level of DC leak current was measured and plotted in the below graph

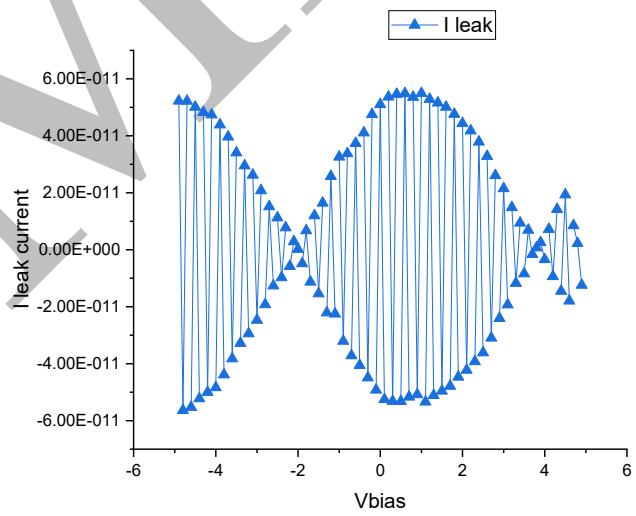


Figure 14. plot of DC bias voltage V/s DC leak current

The level of leakage was found to be approximately 50pA which is low. The two QSCV measurements was with leak compensation OFF and ON method. It was found from the graph that the leak compensation OFF graph was pretty noisy and leak compensation ON graph was found much accurate without any noise. All the measurements has to be done with leak compensation ON.

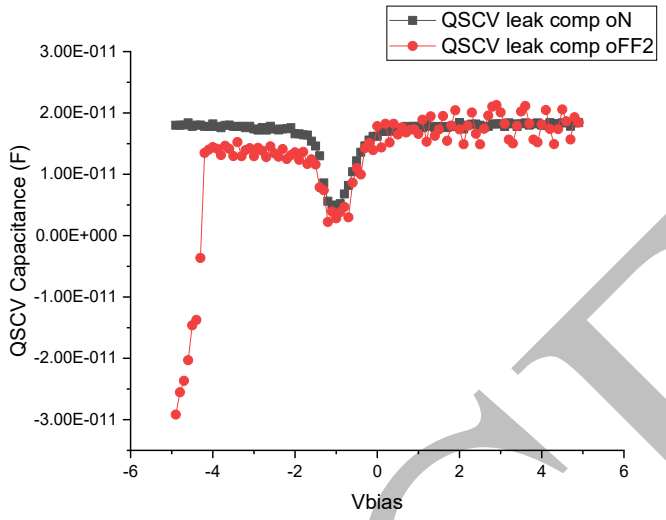


Figure 15. plot of DC bias voltage V/s QSCV with and without leak compensation method

— Set appropriate integration time for the leak measurement:

The parameter of Integ_L is the integration time for the leak current measurement. The leak current is subtracted from the charge current during the C integration time at each CV sweep step. This feature provides the accurate QSCV data by eliminating the effect of leak current for leaky device, but it could add the unexpected error by noise from the device and SMU, unless it is appropriately set up.

Obviously the unstable leak current measurement results in unstable QSCV data, because the leak current is subtracted from the charge current of QSCV measurement. From this viewpoint, the leak measurement must be accurate enough and low noise relatively to the QSCV charge current measurement. Hence, it is recommended to use the 1 PLC (power line cycle) averaging for the integration time for leak current (Integ_L). Using the PLC multiplied integration time can reduce the power line oriented noise drastically.

How to reduce the noise in the QSCV measurement

— Increase ΔV for QSCV measurement:
When the measurement data is noisy, try to use larger ΔV. Since the amount of charge and its transient current are defined by the ΔV, larger ΔV induces larger charge current and it improves the signal to noise ratio. The ΔV of 100 mV or 200 mV would be a good starting point for the QSCV measurement for most of cases.

— Use the SMU at gate for QSCV measurement:

To measure the MOScap, two SMU are used in the QSCV measurements as shown in Figure 16. SMU 4 is connected to the gate and SMU 3 is connected to the substrate. To reduce the noise, it is recommended to use the SMU at gate site for the current measurement for QSCV. The gate side is usually high impedance and less affected by the noise from the measurement environment.

— Choose the SMU to sweep the voltage:

Whichever SMU connected to the gate or substrate can be a voltage sweep source. However, it is important to note that the effect of the stray capacitance Cg or Cs, as shown in Figure 16. In Figure 16(a), the voltage is swept and the charge current is also measured at gate side. In addition to the charge current to the device, the charge current (Is) into the stray capacitance (Cg) is also measured. This can be a measurement error. In Figure 16(b), on the other hand, there is no charge current into the stray capacitance (Cg), because the voltage remains the same at the gate side. Although these stray capacitance components can be cancelled by the offset capacitor compensation, it is recommended to choose the SMU to sweep the voltage carefully. In general, it is recommended to measure the QSCV at gate and sweep the voltage at substrate, as shown in Figure 16(b).

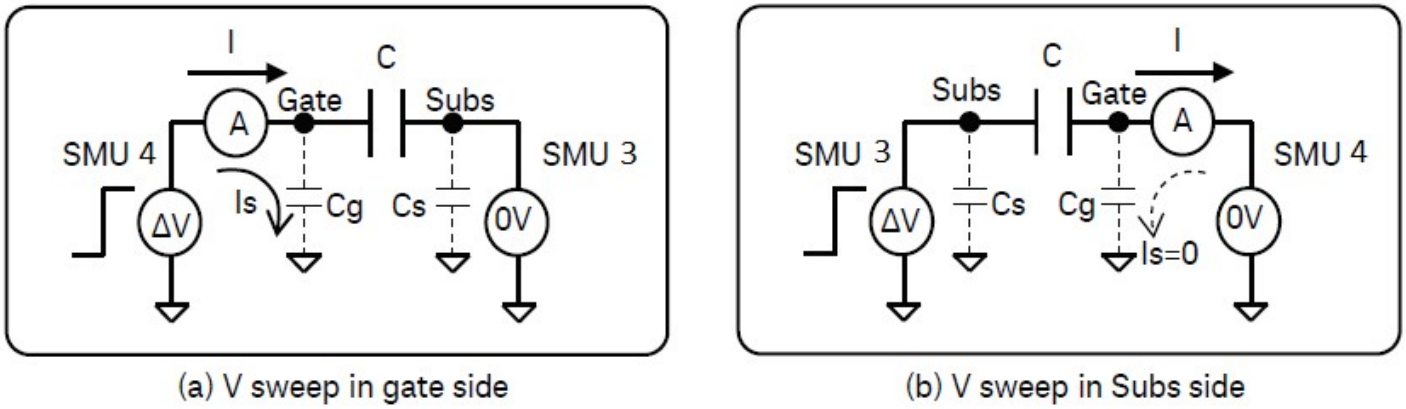


Figure16. Effect of the charge current into stray capacitance [2]

To find out the interface trap density, measurements was done to the following sample

Sample details

Sample : Moscap

Oxide: Sio2 with thickness of 50nm

Substrate : N- type silicon

Experiment details

1) High frequency capacitance verses voltage sweep was done at 1Mhz with Dc bias voltage of -5 to +5V and AC oscillation voltage of 30mV.

2) QSCV measurement was done with the following details

t_{Hold} (s)	t_{Delay} (s)	$t_{\Delta Q,int}$ (s)	t_{leak} (s)	V_{Start} (V)	V_{Stop} (V)	V_{Step} (V)	$V_{QSCV,Step}$ (V)	I_{Comp} (mA)	I_{Meas} (nA)
5	5	1.5	0.2	-5	5	0.1	0.005	10	10

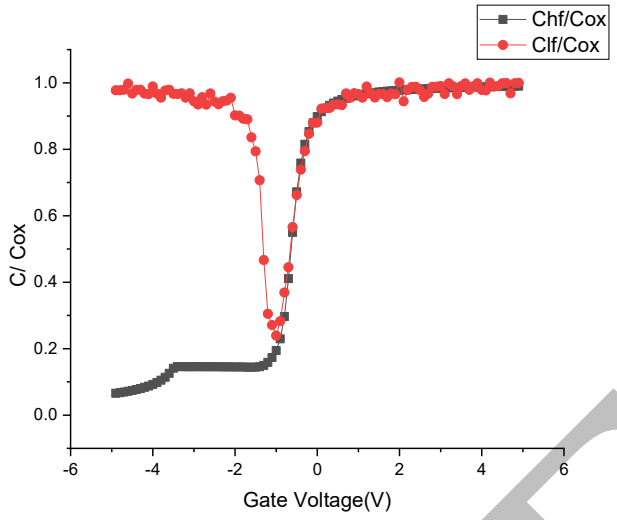


Figure 17: High and low frequency CV curves

This application note describes the change in capacitance of a metal oxide semiconductor (MOS) capacitor measured at a high frequency as a function of bias voltage at room temperature. The interface traps which are measured at a high frequency do not respond but do respond at low frequency with slowly varying bias voltage. The interface traps act as fixed charge and the resulting shift in high-frequency *C–V* curve gives the true evidence of interface trap density at the interface of SiO2. On the other hand, Berglund integral equation showed that interface trap density can be determined by comparing the theoretical *C–V* curve to experimental low-frequency curve because interface traps do respond at low frequency.

The interface trap density was calculated using the following formula

$$D_{\mathrm{it}} = \frac{C_{\mathrm{ox}}}{q}\left(\frac{C_{\mathrm{LF}}/C_{\mathrm{ox}}}{1-C_{\mathrm{LF}}/C_{\mathrm{ox}}} - \frac{C_{\mathrm{HF}}/C_{\mathrm{ox}}}{1-C_{\mathrm{HF}}/C_{\mathrm{ox}}}\right) \mathrm{cm}^{-2}\,\mathrm{eV}^{-1}.$$

The calculated density of interface trap states v/s gate bias voltage is presented in figure18.

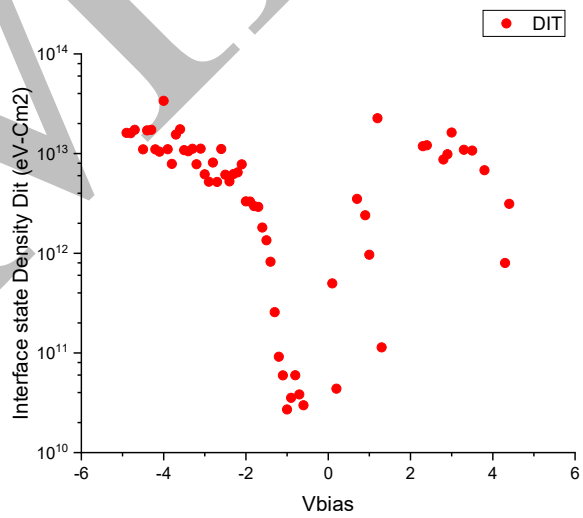


Figure 18: Interface trap density obtained from high low frequency CV vs. Gate Bias Voltage

It was found out to be ~ 10^{13} $cm^{-2}eV^{-1}$. However, using this method, trap states near the conduction band and valance band could be probed. The gate bias voltage was converted to surface potential and further to energy level with respect to conduction band minima using the Berglund integral, described using the following equation.

$$\Psi_s = \int_{V_{g1}}^{V_{g2}} (1 - C_{lf}/C_{ox})\, dV_g + \Delta$$

The surface potential vs. gate voltage plot is shown in figure. 19. The distribution of interface trap density versus energy level with respect to the valence band and conduction band is shown in the figure 20.

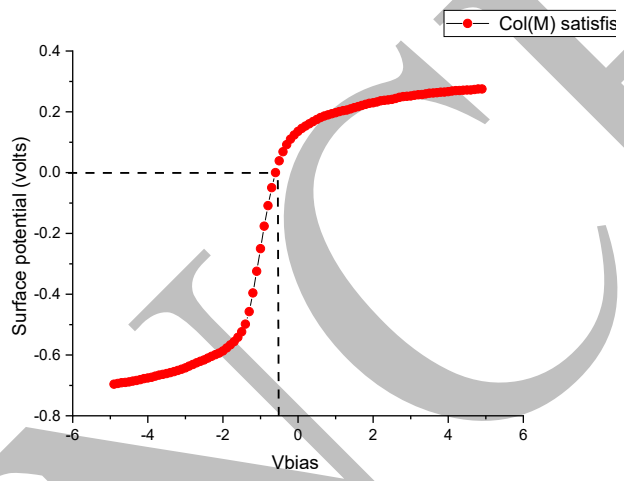


Figure 19: Surface Potential vs. Gate Bias

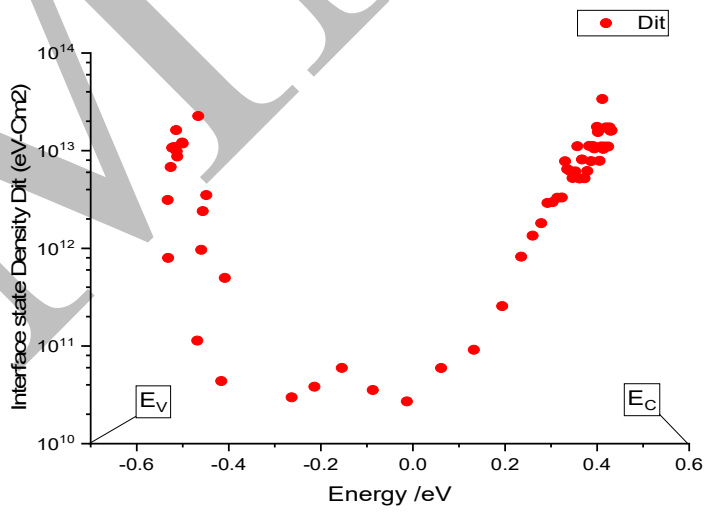


Figure 20: Trap energy level vs. Interface trap density

References:

1) Variation of interface trap level charge density within the bandgap of 4H-SiC with varying oxide thickness Sanjeev k gupta1,2, A Azam2 and Jakhtar1

2) http://literature.cdn.keysight.com/litweb/pdf/5992-0436EN.pdf

3) A book on Semiconductor Material and Device characterization, third edition Dieter. K. Schroder